

REMARKS

Reconsideration and withdrawal of the rejections set forth in the Office Action dated February 9, 2006, is respectfully requested in view of this amendment. By this amendment, claims 1 and 2 have been amended. Claims 1 and 2 are pending in this application.

Claim 1 has been amended in order to describe the first gate circuit supplying the first row select pulses to the row electrodes so that the display signals are written in a row of pixels. The claim also has been amended to describe a second gate circuit to supply the second row select pulses to the row electrodes of respective horizontal blanking periods of the vertical scan period. Claim 2 has been amended to describe the row driver providing first and second row select pulses. Claim 2, which had described a row driver providing display signals now describes the first period during which a column driver provides display signals. It is respectfully submitted that the above amendments introduce no new matter within the meaning of 35 U.S.C. §132.

Rejections Under 35 U.S.C. §112

In the outstanding Office Action, the Examiner rejected claim 1 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

Response

Reconsideration and withdrawal of the rejection are respectfully requested. By this Response and Amendment, the rejections to claim 1 is respectfully traversed. It is respectfully submitted that the claim limitation, "a second shift register to sequentially generate and supply second row select pulses that reset pixels to a reset voltage to the row electrodes, in part or in whole, of respective horizontal blanking periods of the vertical scan period in response to a second scan start signal" is fully explained and described in the specification. The specification clearly describes this, at page 7, line 26 to page 10, line 13 and FIG.3. In addition, the Applicant

amends claim 1 at present in order to more clearly point out the subject matter of the present invention. Specifically, the applicant amends claim 1 to include first and second gate circuits that provide the row electrodes with the row select pulses.

Rejections Under 35 U.S.C. §103

Claim 1 is rejected under 35 U.S.C. §103(a) as being unpatentable over Edwards et al. (US Pub.No.2003/0016202 A1) in view of Imamura (US. Pub.No.2002/0011994 A1).

Claim 2 is rejected under 35 U.S.C. §103(a) as being unpatentable over Edwards et al. and Imamura as applied to claim 1 above, and further in view of Kondoh (US Pub.No.2002/0158831 A1) .

Response

Reconsideration and withdrawal of the rejection are respectfully requested.

Applicant's claim 1 describes:

"... column ... row electrodes being orthogonal to the column electrodes ... pixels arranged in a matrix at intersections of the column and row electrodes.. a column driver ... a row driver ... comprising ... a first shift register ... [generating] row select pulses ... a first gate circuit ... [supplying] ... row select pulses ... so that the display signals are written in a row of the pixels ... a second shift register ... [generating] second row select pulses that reset pixels to a reset voltage in response to a second scan start signal ... a second gate circuit to supply the second row select pulses to the row electrodes ... respective horizontal blanking periods of the vertical scan period."

Imamura fails to show or suggest the use of the first and second shift registers to generate the row select pulses for resetting the pixels and to provide row select pulses.

Imamura describes a first shift register and a second shift register in FIG. 10A. These registers, however, do not correspond to a first shift register and a second shift register of the

present invention. Imamura clarifies simultaneous operation in the detailed description, which details a Scan Electrode Drive Circuit (Y Driver) in paragraph [0085], *et seq.* As described in paragraph [0086], the two registers in FIG.10A are provided to realize a method, namely a multiple line selection derive method, in which plural lines are simultaneously driven. Therefore, the two shift registers in Imamura are equivalent to registers obtained by dividing the first shift register of the present invention.

Imamura does not teach or suggest any constitution equivalent to a second shift register and a second gate circuit for providing row electrodes with second row select pulses that reset pixels to a reset voltage, in part or in whole, of respective horizontal blanking periods of the vertical scan period.

Accordingly, the claims, as amended, clearly distinguish the present invention over the prior art of record.

Claim 2 further defines the level setter configured to set a horizontal blanking period as a period to provide the reset voltage. The claim further defines the output unit controlling all switches of the column driver in a reset period in cooperation with the level setter, and the row driver providing the first and second row select pulses to select the row electrodes one after another. The pulses are described as provided for each horizontal scan period so that the output unit provides the column electrodes with the reset voltage such that an absolute value of voltage accumulated in each pixel due to the display signal is below a predetermined value in each vertical scan period. These features are neither shown nor suggested by the prior art of record. Specifically, Edwards, Imamura and Kondoh fail to suggest the provision of the pulses in the manner set forth in claim 2. Accordingly, claim 2 is patentably novel under 35 U.S.C. §103(a).

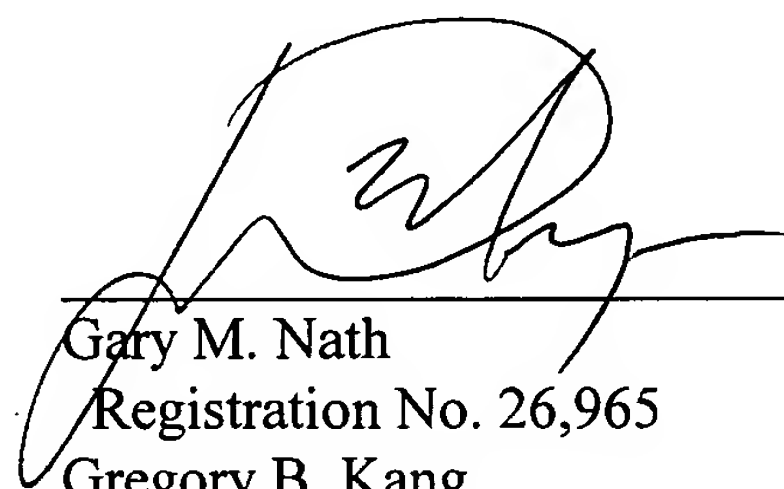
CONCLUSION

In light of the foregoing, Applicants submit that the application is in condition for allowance. If the Examiner believes the application is not in condition for allowance, Applicants respectfully request that the Examiner call the undersigned.

Respectfully submitted,
NATH & ASSOCIATES PLLC

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NATH & ASSOCIATES PLLC
112 South West Street
Alexandria, VA 22314-2891
Tel: 703-548-6284
Fax: 703-683-8396



Gary M. Nath
Registration No. 26,965
Gregory B. Kang
Registration No. 45,273
Jerald L. Meyer
Registration No. 41,194
Stanley N. Protigal
Registration No. 27,658